AMENDMENTS

Please enter the following amendments:

In the Specification

Please add the following paragraph beginning on page 1, line 5:

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation application, which is based on and claims priority to

U. S. Utility Patent Application 10/055,299, filed on January 23, 2002, and which is

incorporated herein in its entirety.

In the Claims

Please amend the claims as follows:

1. – 20.   (Canceled)

21.   (Newly Added) A computer system comprising:

a memory having a magnetic tunnel junction (MTJ) memory device, the MTJ memory

device having a memory cell;

a biasing circuit configured to supply at least two different biasing voltages to the cell;

a sensing circuit configured to measure the current flowing through the cell at each of

the at least two different biasing voltages; and

a processing element configured to determine a ratio of the current flowing through the

cell at a first one of the at least two different biasing voltages to the current flowing through the

cell at a second one of the at least two different biasing voltages and to compare the ratio to a

predetermined value.

22.   (Newly Added) The system of claim 21, wherein the biasing circuit, the sensing circuit, the processing element and the MTJ device are fabricated as an application specific integrated circuit (ASIC).

23.   (Newly Added) The system of claim 21, wherein the biasing circuit is a voltage supply.

24.   (Newly Added) The system of claim 21, wherein the sensing circuit is an ammeter.

25.   (Newly Added) The system of claim 21, further comprising a reference MTJ memory cell having a known state.

26.   (Newly Added) The system of claim 21, wherein the MTJ device is a magnetic random access memory (MRAM).

27.   (Newly Added) The system of claim 21, wherein the MRAM is an MRAM array.

28.   (Newly Added) The system claim 21, wherein the second bias voltage is less than the first bias voltage.

29.   (Newly Added) The system of claim 21, wherein the second bias voltage is more than the first bias voltage.

30. (Newly Added) The system of claim 21, wherein the second bias voltage is on the order of 1/3 of the first bias voltage.

31. (Newly Added) The system of claim 21, further comprising a processor operative to execute instructions stored in said memory.

32. (Newly Added) A method for determining the logic state of a memory cell in a magnetic tunnel junction (MTJ) memory device, comprising:

applying a first bias voltage to the cell;

measuring a current flowing through the cell at the first bias voltage;

applying a second bias voltage to the cell, the second bias voltage being different from the first bias voltage;

measuring a current flowing through the cell at the second bias voltage;

using the current flowing through the cell and measured at each of the first bias voltage and second bias voltage to determine the logic state of the cell.

33. The method of claim 32, wherein the second bias voltage is less than the first bias voltage.

34. The method of claim 32, wherein the second bias voltage is greater than the first bias voltage.

35. The method of claim 32, wherein the second bias voltage is on the order of 1/3 of the first bias voltage.

36.   The method of claim 32, wherein the MTJ device is a magnetic random access memory (MRAM).

37.   The method of claim 32, wherein the MRAM is an MRAM array.